CLAIMS:

1. A method of forming circuitry comprising:

forming a capacitor electrode over one region of a substrate:

forming a capacitor dielectric layer proximate the electrode;

providing a conductive diffusion barrier layer between the electrode and the capacitor dielectric layer;

forming a conductive plug over another region of the substrate, the conductive plug comprising a same material as the conductive diffusion barrier layer; and

at least a portion of the conductive plug being formed simultaneously with the conductive diffusion barrier layer.

2. The method of claim 1 wherein the conductive diffusion barrier layer comprises a metal nitride.

3. The method of claim 1 wherein the electrode is a storage node of the capacitor.

4. The method of claim 1 wherein the conductive plug is formed within an opening in an insulative layer and wherein the capacitor electrode is at least a portion of a capacitor cell plate, the method further comprising:

before forming the capacitor electrode, forming a storage node of the capacitor and forming the capacitor dielectric layer over the storage node;

forming a protective layer over the capacitor dielectric layer before forming the opening in the insulative layer;

protecting the capacitor dielectric layer with the protective layer while forming the opening in the insulative layer; and

removing the protective layer before forming the conductive diffusion barrier layer.

5. A method of forming circuitry comprising the following steps:

providing a substrate;

defining a memory array region of the substrate and a peripheral region of the substrate, the peripheral region being peripheral to the memory array region;

forming a capacitor construction over the memory array region of the substrate, the capacitor construction comprising a storage node, a capacitor dielectric layer, a capacitor barrier layer and a cell plate layer; the capacitor dielectric layer separating the storage node from the cell plate layer, the capacitor barrier layer separating the capacitor dielectric layer from one of the storage node and the cell plate;

forming an electrical interconnect over the peripheral region and in electrical connection with a doped region, the electrical interconnect comprising a conductive interconnect barrier layer and a metal layer, the conductive interconnect barrier layer being between the doped region and the metal layer; and

wherein the conductive interconnect barrier layer and capacitor barrier layer are formed in a same step.

6. The method of claim 5 wherein the capacitor barrier layer and conductive interconnect barrier layer comprise TiN.

7. The method of claim 5 wherein the capacitor barrier layer and conductive interconnect barrier layer comprise TiN, and wherein the same step comprises chemical vapor deposition.

8. The method of claim 5 wherein the capacitor barrier layer and conductive interconnect barrier layer comprise TiN, and wherein the metal layer comprises one or more of Ti, W, Al and Cu.

9. A method of forming circuitry, comprising:

providing a substrate;

defining a memory array region of the substrate and a peripheral region of the substrate, the peripheral region being peripheral to the memory array region;

forming a capacitor construction over the memory array region of the substrate, the capacitor construction comprising a storage node, a capacitor dielectric layer and a cell plate layer; the capacitor dielectric layer separating the storage node from the cell plate layer;

forming an electrical interconnect over the peripheral region, the interconnect being electrically connected to the cell plate layer; and

at least a portion of the interconnect being formed during formation of the cell plate layer.

10. The method of claim 9 wherein the forming the interconnect and the cell plate layer comprises deposition of a common and continuous conductive material over the peripheral and memory array regions of the substrate.

11. The method of claim 9 wherein the interconnect extends between the cell plate layer and the substrate to electrically connect the cell plate layer to a node elevational below the cell plate layer.

12. The method of claim 9 wherein the interconnect extends from the cell plate layer to the substrate to electrically connect the cell plate layer to a node within the substrate.

13. A method of forming circuitry, comprising:

providing a substrate;

defining a memory array region of the substrate and a peripheral region of the substrate, the peripheral region being peripheral to the memory array region;

defining a first electrical node proximate the memory array region of the substrate, and defining a second electrical node proximate the peripheral region of the substrate;

forming an electrically insulative layer over the substrate and over the electrical nodes;

forming a first opening through the electrically insulative layer;

forming at least a portion of a capacitor storage node within the first opening and in electrical connection with the first electrical node;

forming a second opening through the electrically insulative layer to the second electrical node;

in a common deposition step, forming a conductive material over the storage node and within the second opening in electrical connection with the second node; and

forming a capacitor dielectric layer and a capacitor electrode operatively adjacent the storage node, one of the storage node or the capacitor electrode comprising the conductive material.

14. The method of claim 13 further comprising:

forming a first layer over the storage node layer and over the insulative layer before etching the second opening; and

etching the second opening through the first layer.

15. The method of claim 14 wherein the first layer comprises at least one of TiN and WN.

16. The method of claim 14 wherein the first layer comprises TiN.

17. The method of claim 14 further comprising forming the capacitor dielectric layer over the storage node layer before forming the first layer.

18. The method of claim 14 further comprising:

defining a third electrical node proximate the substrate, the third electrical node being proximate the peripheral region;

forming the electrically insulative layer over the third electrical node;

simultaneously etching the second and third openings through the first layer and through the insulative layer to the second and third electrical nodes, respectively; and

in the common deposition step, forming the conductive material within the third opening.

19. The method of claim 13 wherein a portion of the conductive material overlies the insulative layer proximate the second opening, the method further comprising:

forming a protective layer over another portion of the conductive material that is over the storage node layer; and

after forming the protective layer, removing the portion of the conductive material that overlies the insulative layer proximate the second opening.

20. The method of claim 13 wherein the conductive material fills the second opening to form a conductive plug within the second opening, the method further comprising:

forming the capacitor dielectric layer over the storage node layer;

forming a metal layer over the conductive plug and over the storage node layer, the capacitor dielectric layer being between the metal layer and the storage node layer, the metal layer comprising at least a portion of the cell electrode layer; and

patterning the metal layer to electrically separate a segment of the metal layer comprising at least the portion of the cell electrode layer from a segment overlying the conductive plug.

21. The method of claim 13 wherein the conductive material fills the second opening to form a conductive plug within the second opening, the method further comprising:

forming the capacitor dielectric layer over the storage node layer; and

forming a metal layer over the conductive plug and over the storage node layer, the capacitor dielectric layer being between the metal layer and the storage node layer, the metal layer comprising at least a portion of the cell electrode layer and being electrically connected to the second electrical node through the conductive plug.

22. The method of claim 13 further comprising forming the capacitor dielectric layer over the storage node layer prior to etching the second opening.

23. The method of claim 13 wherein the substrate comprises monocrystalline silicon and the electrical nodes comprise electrically conductive diffusion regions formed within the substrate.

24. The method of claim 13 wherein the forming the conductive material comprises forming a metal-comprising layer over the storage node layer and within the second opening.

25. The method of claim 13 wherein the forming the conductive material comprises forming at least two layers over the storage node layer and within the second opening.

26. The method of claim 13 wherein the forming the conductive material comprises forming at least three layers over the storage node layer and within the second opening.

27. The method of claim 13 wherein the forming the conductive material comprises:

forming a layer comprising TiN over the storage node layer and within the second opening; and

forming a second layer over the layer comprising TiN, the second layer not comprising TiN.

28. The method of claim 13 further comprising:

defining a third electrical node proximate the substrate;

forming the electrically insulative layer over the third electrical node;

etching a third opening through the insulative layer and to the third electrical node while etching the second opening through the electrically insulative layer; and

in the common deposition step, forming the conductive material within the third opening.

29. The method of claim 28 wherein the second and third nodes are electrically connected through a transistor.

30. An integrated circuit comprising:

a capacitor and a conductive plug, the conductive plug and capacitor comprising a first common and continuous layer.

31. The integrated circuit of claim 30 wherein the first common and continuous layer comprises TiN.

32. The integrated circuit of claim 30 wherein the conductive plug and capacitor further comprise a second common and continuous layer over the first common and continuous layer.

33. The integrated circuit of claim 32 wherein the first common and continuous layer comprises a metal nitride and the second common and continuous layer comprises a metal, the second common and continuous layer being chemically different than the first common and continuous layer.

34. The integrated circuit of claim 30 wherein the conductive plug and capacitor further comprise:

a second common and continuous layer over the first common and continuous layer; and

a third common and continuous layer over the second common and continuous layer.

35. The integrated circuit of claim 34 wherein the first common and continuous layer comprises Ti, the second common and continuous layer comprises a metal nitride, and the third common and continuous layer comprises one or more of W, Al and Cu; the first, second and third common and continuous layers being chemically different from one another.

36. The integrated circuit of claim 30 further comprising:

a substrate;

an insulative layer over the substrate;

the conductive plug extending through the insulative layer;

the capacitor comprising a storage node extending through the insulative layer and a cell electrode over the insulative layer; and

the cell electrode comprising the first common and continuous layer.

37. The integrated circuit of claim 36 wherein the first common and continuous layer comprises TiN.

38. The integrated circuit of claim 36 wherein the conductive plug and the electrode layer further comprise a second common and continuous layer over the first common and continuous layer.

39. The integrated circuit of claim 36 wherein the conductive plug and cell electrode further comprise:

a second common and continuous layer over the first common and continuous layer; and

a third common and continuous layer over the second common and continuous layer.

40. A circuit construction comprising:

a substrate having a memory array region and a peripheral region that is peripheral to the memory array region;

a capacitor construction over the memory array region of the substrate, the capacitor construction comprising a storage node, a capacitor dielectric layer and a cell plate layer; the capacitor dielectric layer being between the storage node and the cell plate layer; and

an electrical interconnect over the peripheral region, the interconnect being electrically connected to the cell plate layer and extending between the cell plate layer and the substrate.

41. The circuit construction of claim 40 wherein the electrical interconnect extends from the cell plate layer to the substrate.

42. The circuit construction of claim 40 further comprising a transistor proximate the peripheral region of the substrate, the transistor comprising a source/drain region, the electrical interconnect extending from the cell plate layer to the source/drain region.

43. The circuit construction of claim 40 wherein the electrical interconnect and cell plate layer comprise at least one common and continuous layer.

44. The circuit construction of claim 40 wherein the electrical interconnect and cell plate layer comprise at least two common and continuous layers.

45. The circuit construction of claim 40 wherein the electrical interconnect and cell plate layer comprise at least three common and continuous layers.